A COMPUTER-AIDED APPROACH TO THE NONLINEAR DESIGN OF MICROWAVE TRANSISTOR OSCILLATORS

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Summary

The design of microwave transistor oscillators is tackled by modern nonlinear network techniques. The result is a general computer-aided approach providing cost-effective MIC designs and full numerical description of circuit performance.

Introduction

This paper describes a general computer approach to the design of transistor oscillators for use at microwave frequencies. Its only assumption -the availability of a nonlinear model for the active device- can be considered a reasonable one in view of the work of several research teams (e.g., [1÷3]), and is further checked here by experiments that were carried out on a 500 mW microstrip oscillator. Otherwise the formulation is rigorous, at least in principle.

The design method described here is more advanced than most previous approaches to the same problem under several respects. As a first point, the harmonics of the output frequency are systematically accounted for, so that the well-known limitations of design techniques based on large-signal S parameters [4-5] are overcome. This may be of special importance in the case of power devices acting in a frequency-selective environment such as microstrip circuitry. Furthermore a straightforward computer solution of the basic problem -designing an oscillator of given frequency having the maximum possible output power (or efficiency)- becomes feasible and cost-effective thanks to a new optimization strategy. The unknown circuit parameters and the signal waveforms are simultaneously determined by minimizing a unique objective function, thus avoiding the nesting of nonlinear analysis and network optimization loops. Finally the use of perturbation techniques leads to a quantitative analysis of some aspects of circuit performance -such as steady-state stability and spurious oscillations- which are normally treated by empirical approaches [6].

Design method

Fig. 1 gives a general representation of the oscillator circuit to be dealt with. $\mathcal{N}$ is a linear network containing all passive circuitry as well as the transistor package parasitics and the linear elements (if any) of the chip equivalent circuit. The bias generator and load are put into evidence in the figure. Generally speaking the chip is a three-terminal nonlinear network, and is mathematically described as a nonlinear two-port, taking one of the terminals as a reference. This is illustrated in fig. 2 for a particular bipolar n-p-n chip, the MSC 3000, whose equivalent circuit is discussed in detail in [3].

The time-domain nonlinear equations of the intrinsic chip can be written in the vector form (see fig. 2 as an example):

$$\underline{i} = \underline{f}\left(\underline{i}, \frac{d\underline{i}}{dt}, \underline{v}, \frac{d\underline{v}}{dt}\right) \qquad (1)$$

where all underlined symbols denote two-element vectors, e.g., $\underline{i} = \left[i_1 \;\; i_2\right]^T$ (^{T} denotes transposition). Now let us assume that a periodic steady-state oscillation with a fundamental frequency f_0 takes place in the network. If N is the number of significant harmonics (including the fundamental), we will have

$$\underline{i}(t) = \mathrm{Re}\left\{\sum_{k=0}^{N} \underline{I}_k \exp(j\,k\,\omega_0\,t)\right\}$$
$$\underline{v}(t) = \mathrm{Re}\left\{\sum_{k=0}^{N} \underline{V}_k \exp(j\,k\,\omega_0\,t)\right\} \qquad (2)$$

where $\underline{I}_k$, $\underline{V}_k$ are complex two-element vectors, e.g., $\underline{I}_k = \left[I_{1k} \;\; I_{2k}\right]^T$. The electrical regime described by (2) must satisfy the constraints imposed by the linear network, that is,

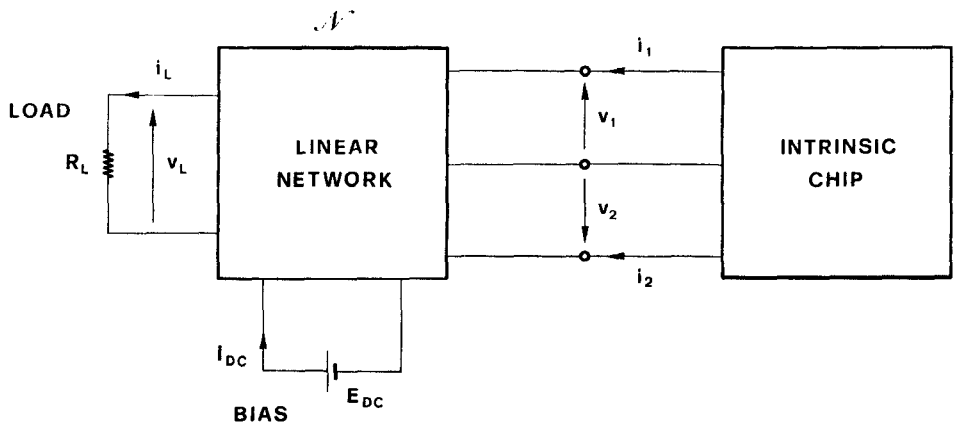

Fig. 1 - Schematic oscillator topology.

$$\underline{I}_k = \underline{Y}(k\,\omega_0)\,\underline{V}_k + \underline{J}_k \qquad (3)$$

where $\underline{Y}(\omega)$ is the admittance matrix of the linear two-port "seen" by the chip; $\underline{J}_k \neq 0$ for $k = 0$ only in the

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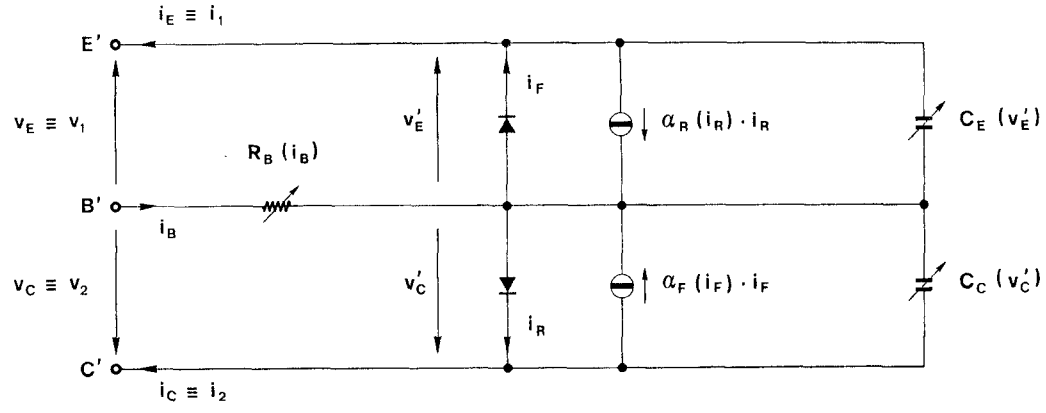

Fig. 2 - Microwave transistor chip equivalent circuit.

case of a free-running oscillator, and for k = 0, k = 1 in the case of an injection-locked source. By means of (2) and (3), the right-hand side of (1) becomes a periodic function of time of period $1/f_0$, also depending on the voltage harmonics. Thus we write

$$\underline{i}(t) = \mathrm{Re}\left\{\sum_{k=0}^{N} \underline{F}_k(\underline{V}) \exp(j\, k\, \omega_0\, t)\right\} \tag{4}$$

where $\underline{V}$ denotes the vector of all voltage harmonics and the $\underline{F}_k(\underline{V})$ are computed by the Fast-Fourier-Transform algorithm.
Combining (4) with (2) and (3) we obtain the solving system

$$\begin{cases} \underline{F}_k(\underline{V}) - \underline{Y}(k\,\omega_0)\,\underline{V}_k = \underline{J}_k \\ k = 0, 1 \ldots N \end{cases} \tag{5}$$

The network and its electrical regime (described by the vector $\underline{V}$) must satisfy (5) and a set of additional constraints arising from the design specifications. The quantities of interest are usually the power output P_L at the fundamental and/or the circuit efficiency η, as well as the harmonic suppression S at the load. Referring to fig. 1, let V_{Lk} be the kth load-voltage harmonic (k = 1, 2 ... N); then we have

$$P_L = \frac{|V_{L1}|^2}{2\,R_L} \qquad \eta = \frac{P_L}{E_{DC}\,I_{DC}}$$

$$S = 10\,\log_{10}\frac{|V_{L1}|^2}{\sum_{k=2}^{N}|V_{Lk}|^2}\,. \tag{6}$$

A typical set of design specifications can be of the form

$$\begin{cases} S > S_{min} \\ P_L \text{ or } \eta \text{ "as large as possible"}, \end{cases} \tag{7}$$

the amount of "available" power being *a priori* unknown.

Note that (5) is a nonhomogeneous system of 2(2N + 1) nonlinear real equations. Since ω_0 is known as a design specification, the real unknowns explicitly appearing in (5) are only 4N + 1, because the phase of one of the voltage harmonics may be chosen arbitrarily. Thus for the problem to be numerically well-conditioned, one additional degree of freedom is required, such as a free parameter in the linear network. Further design parameters must be available in order to meet a set of electrical specifications, such as (7). In general, it is essential that bias-circuit parameters be included in the set of design variables, since they usually have a major influence on oscillator performance.

In summary the problem to be solved consists of finding the voltage harmonics and the unknown parameters of the linear network in such a way that (5) and (7) are simultaneously satisfied. In our present approach this problem is reduced to minimizing a suitable objective function F_{OB} and is solved numerically by conventional optimization routines. To define the objective we first introduce the harmonic-balance error

$$e_B = \sqrt{\sum_{k=0}^{N} \left| \underline{F}_k(\underline{V}) - \underline{Y}(k\,\omega_0)\,\underline{V}_k - \underline{J}_k \right|^2} \tag{8}$$

The only physically acceptable solutions are those yielding $e_B = 0$. However, for all practical purposes this condition can be replaced by $e_B < e_{max}$, where e_{max} is a suitable threshold value to be established by experience in relation with the given problem. A consistent choice has been found to be $e_{max} = I/1000$, I representing the collector (or drain) bias current. We now define the weighted errors

$$\begin{aligned} E_B &= W_B \cdot (e_B - e_{max}) \\ E_P &= W_P \cdot (P_{min} - P_L) \\ E_S &= W_S \cdot (S_{min} - S) \end{aligned} \tag{9}$$

where the W's are positive quantities and P_{min} represents the minimum acceptable output power, and let

$$E = \max(E_B, E_P, E_S) \tag{10}$$

The objective function is expressed in the form

$$F_{OB} = \begin{cases} \sqrt{\sum_i^{+} E_i^2} & \text{if } E > 0 \\ E_P & \text{if } E < 0 \end{cases} \qquad (11)$$

where i = B, P, S and the $\sum^{+}$ is only extended to *positive* errors.
When E < 0 the harmonic-balance requirement is numerically satisfied and so is the specification on harmonic suppression, so that the efforts of the optimization algorithm are entirely devoted to decreasing E_P, that is, increasing the output power. On the contrary, if one of the imposed bounds P_{min}, S_{min} is too large, the optimization ends with a positive F_{OB} and usually with e_B still too large for the results to be physically acceptable.

A final point concerns junction temperature. In general, in the equivalent circuit of the chip there appear temperature-dependent parameters, such as the diode saturation currents in the model of fig. 2. For power devices this dependence must be taken into account since temperatures of 80°C or more are easily reached in CW operation. To do this, prior to each function evaluation we find the current estimate of the junction temperature in the form

$$T_j = R_{TH} \cdot \left\{ - \underline{V}_0^T \underline{I}_0 - \frac{1}{2} \sum_{k=1}^{N} \mathrm{Re} \left(\underline{V}_k^T \underline{I}_k^* \right) \right\} + T_a \qquad (12)$$

where R_{TH} is the thermal resistance of the chip and T_a is room temperature. (12) is used to define all temperature-dependent quantities in the chip model. After a successful optimization has been carried out, T_j represents the actual temperature of the chip, so that the nonlinear constraints imposed by the device are correctly formulated in relation to its physical conditions of operation.

A design example

In this section we report a few experimental results concerning a medium-power low-noise oscillator that was designed according to the method previously described. The oscillator had to be mechanically tunable over the 2250 ÷ 2500 MHz band with a minimum output power of 500 mW and a harmonic content at least 20 dB below the fundamental. The transistor chip selected was an MSC 3001, corresponding to two MSC 3000 connected in parallel; this chip was included in a conventional grounded-bar package for which an accurate circuit model was available. Mainly for the sake of thermal dissipation a common-collector configuration was adopted. In order to meet the tuning and noise requirements, a tunable coaxial cavity was used and was connected to the transistor base via a capacitive coupling and a microstrip transformer; this also allowed a tuning varactor to be coupled to the oscillator, when required, without perturbing the cavity and thus with minimum noise degradation. On the emitter side the transistor was matched to the load by a very simple stub matching network realized in microstrip.

The design was carried out by optimizing all essential electrical parameters of the passive network (including the bias circuit) as well as three harmonics besides the fundamental and D.C. components. The results of a conventional small-signal design (e.g., [7]) provided a suitable starting point. In order to account properly for the behavior of the passive circuit at the higher harmonics, the measured propagation constants of the microstrip lines (i.e., including attenuation and dispersion) as well as the equivalent circuits of the discontinuities were used in all calculations.
The nominal design was produced by use of the nonlinear model of one specific MSC 3000 chip (given in [3]) and predicted an output power ranging from 530 to 560 mW across the band of interest with a minimum efficiency of 25% and a harmonic suppression at the load larger than 26.5 dB. The bias voltage (established by system requirements) was -16 V. The reliability of this design was checked by dropping the nonlinear model of a different chip (also given in [3]) into the same passive circuit, and showing that no significant degradation of the oscillator performance would occur in this way. Several tens of similar oscillators were then built (for production purposes) and were found to behave in very close agreement with the predicted performance after minor adjustments of the emitter bias resistor and of the cavity coupling capacitance only.

The above results suggest that the use of accurate large-signal models of the active devices and of sophisticated CAD techniques might well be worthwhile for removing the considerable amounts of guesswork and empirical trimming which are still required by the design of microwave oscillators and other classes of nonlinear microwave subsystems.

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